NAME

ext2sim – convert hierarchical *ext*(5) extracted-circuit files to flat *sim*(5) files

SYNOPSIS

ext2sim [**–a** *aliasfile*] [**–l** *labelsfile*] [**–o** *simfile*] [**–A**] [**–B**] [**–F**] [**–L**] [**–t**] [*extcheck-options*] *root*

DESCRIPTION

Ext2sim will convert an extracted circuit from the hierarchical *ext*(5) representation produced by Magic to the flat *sim*(5) representation required by many simulation tools. The root of the tree to be extracted is the file *root***.ext**; it and all the files it references are recursively flattened. The result is a single, flat representation of the circuit that is written to the file *root***.sim**, a list of node aliases written to the file *root***.al**, and a list of the locations of all nodenames in CIF format, suitable for plotting, to the file *root***.nodes**. The file *root***.sim** is suitable for use with programs such as *crystal*(1), *esim*(1), or *sim2spice*(1).

The following options are recognized:

–a*aliasfile* Instead of leaving node aliases in the file *root***.al**, leave it in *aliasfile*.

–l*labelfile* Instead of leaving a CIF file with the locations of all node names in the file *root***.nodes**, leave it in *labelfile*.

–o*outfile* Instead of leaving output in the file *root***.sim**, leave it in *outfile*.

–A Don't produce the aliases file.

–B Don't output transistor or node attributes in the **.sim** file. This option is necessary when preparing input for programs that don't know about attributes, such as *sim2spice*(1) (which is actually made obsolete by *ext2spice*(1), anyway), or *rsim*(1).

–F Don't output nodes that aren't connected to fets (floating nodes).

–L Don't produce the label file.

–t*char* Trim characters from node names when writing the output file. *Char* should be either "#" or "!". The option may be used twice if both characters are desired.

In addition, all of the options of *extcheck*(1) are accepted.

SCALING AND UNITS

If all of the **.ext** files in the tree read by *ext2sim* have the same geometrical scale (specified in the **scale** line in each **.ext** file), this scale is reflected through to the output, resulting in substantially smaller **.sim** files. Otherwise, the geometrical unit in the output **.sim** file is a centimicron.

Resistance and capacitance are always output in ohms and picofarads, respectively.

SEE ALSO

extcheck(1), ext2dlys(1), ext2spice(1), magic(1), rsim(1), sim2spice(1), ext(5), sim(5)

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BUGS

Transistor gate capacitance is typically not included in node capacitances, as most analysis tools compute the gate capacitance directly from the gate area. The **-c** flag therefore provides a limit only on non-gate capacitance.