ECE 491 Senior Design I Syllabus Fall 2008

Catalog Description

This course uses a data network to introduce students to team project work. Course topics include computer networks from the physical layer to communication protocols. A representative network is designed and realized in the laboratory. Students work in teams; different teams design sub-systems of the network. Lecture/laboratory.

Course Description

This course is the first of a two-semester sequence of senior design projects for ECE majors. Design involves the creation of a system, product, or process that addresses a specific problem or need while meeting a number of *constraints*. While the most obvious constraints are cost, performance, and power, "real" designs must satisfy many additional constraints. For example, a design must often be compatible with similar products or operate using predefined *standards*. A design must be *manufacturable* - it must be possible to realize a design in large volumes in the face of component variation. A design must address concerns about its *environmental impact*, *sustainability*, and its impact on the *health and safety* of the public. And finally, a design must address concerns about its larger *social*, *political*, and *ethical* impact. Because constraints often conflict, it is necessary to compromise and find *tradeoffs* between to reach a solution that is acceptable for the problem the design is intended to address.

In this course you will study the "design process" which engineers use to create designs, undertake a significant design project in a small group, and consider case studies of some successful design projects. You will learn basic concepts in networking and data communications and apply this knowledge in a final design project in which you will implement a wireless network interface using a Field-Programmable Gate Array (FPGA) and the Verilog Hardware Description Language (HDL).

Instructors

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Course Goals

ECE 491 has three major goals:

- 1. Introduce students to the process of designing electronic systems as it is practiced in industry.
- 2. Introduce students to FPGA-based design using the Verilog Hardware Description Language (HDL).
- 3. Introduce ECE Seniors to basic Networking principles with emphasis on the Physical Link and Transport levels.

In addition, the Design Project component of the course is intended to serve as an open-ended "major design experience" that, when combined with the ECE 492 (Senior Design II), satisfies ABET requirements for a "capstone" design experience. The following excerpts from the ABET *Criteria for Accrediting Engineering Programs* summarize these requirements:

"Engineering programs must demonstrate that their students attain:

(c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability"

From ABET Criterion 3 – Program Outcomes and Assessment

"Students must be prepared for engineering practice through the curriculum culminating in a major design experience based on the knowledge and skills acquired in earlier course work and incorporating appropriate engineering standards and multiple realistic constraints." From ABET Criterion 4 – Professional Component

Course Outcomes

To achieve the Course Goals, at the end of this course each student should be able to:

The Design Process:

- 1. Understand the steps of the electronic design process.
- 2. Understand the impact of constraints on design.
- 3. Understand the organization of design teams.
- 4. Understand common tools for project management.
- 5. Understand economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability concerns in electronic design.

Digital System Design with FPGAs and Verilog HDL:

- 6. Understand the general structure of common Field Programmable Gate Arrays (FPGAs).
- 7. Understand the basic constructs of the Verilog Hardware Description Language (HDL).
- 8. Write Verilog code that can be reliably synthesized into combinational logic, sequential logic, and Finite State Machines (FSMs).
- 9. Write a Verilog testbench that verifies the correctness of a design using self-checking procedural code.
- 10. Recognize and avoid common Verilog coding pitfalls.
- 11. Understand the timing of digital systems in FPGA-based systems, especially as they limit clock frequency.
- 12. Understand the purpose of synchronizers in sequential logic designs.
- 13. Understand how handshaking is used to reliably transfer data and control information between sequential circuits operating off different clock signals.

Data Communications and Networking

- 14. Understand simple asynchronous serial communications protocols and create circuits that can interface to these protocols.
- 15. Understand the concept of Manchester encoding for data transmission.
- 16. Understand the protocol of an Ethernet network.
- 17. Understand the layers of the Open Systems Interconnection (OSI) model for networking.

Portions of this course will be used to directly assess the following ECE Department Program Objectives:

- PO1 Have full awareness of and an appetite for life-long learning and understanding of contemporary issues.
- PO2 Have the ability to function in a multi-disciplinary team.
- PO3 Be able to analyze data and communicate results.
- PO4 Be able to solve broad-based engineering problems in a socially-conscious and ethical manner.
- PO6 Be able to design, simulate, build, and test complex digital circuits.
- PO8 Be able to use modern engineering hardware and software tools.

Course Organization

Typical week (day):	
Monday, Wednesday	Lecture
Friday	Occasional quizzes, HW discussion, Design Topics.
Thursday	Laboratory
Typical week (evening section):	
Monday, Wednesday	Lecture
Wednesday	Occasional quizzes, HW discussion, Design Topics.
Thursday	Laboratory

Textbook and Course Materials

- 1. J. Eric Salt and Robert Rothery, Design for Electrical and Computer Engineers, John Wiley, 2002.
- 2. Lecture notes, laboratory experiments, and handouts distributed in class.

Course Website

All course materials will be posted on the Lafayette Moodle course management system (<u>http://moodle.lafayette.edu</u> - log in using your network ID).

Academic Honesty

Students are expected to adhere to the academic honesty guidelines outlined in the Student Handbook. This includes all design work in the laboratory and design projects, which must be performed by each individual lab group. While you may feel free to discuss general approaches and strategies with students in other groups, any sharing of HDL code or other design information is prohibited.

Attendance Policy

Attendance at all lectures and laboratories is required. Excused absences for job interviews, conference travel, etc. must be requested in advance by email describing the reason for your absence and how you will complete the work you missed. For absences from lab, you must also describe how you will balance the lab (or project) workload with your lab partner(s).

Grading

Your numerical grade will be computed using the following weighting:

Final	20%
Quizzes &Homework	20%
Laboratory	30%
Final Project	30%

Laboratory and Project

The laboratory portion of this course is divided into two phases – a set of seven lab experiments in FPGA and data communications design followed by a final design project in which you will design a complete wireless network interface. Because the designs you will be creating will be difficult and open-ended, you will need to work on these both during the scheduled lab session and also **outside** of lab and class. This is particularly true for the final project.

Students will work in groups of two (if there are an odd number of students in a section, one group of three will be allowed in each section). Each group will submit one lab report for each experiment. Lab reports will include a technical memorandum formatted as an Adobe PDF file combined with Verilog code and a number of other deliverables that will be specified in each lab assignment. You will upload each report to Moodle in the form of a compressed ZIP archive. Unless otherwise specified, the deadline for each report is midnight on the night before your lab section is scheduled to begin the next experiment. Lab reports submitted after the deadline will be subject to a 10%/day late penalty.

All students must read and follow the ECE Lab Safety Guidelines posted in the lab.

The primary method of design entry in ECE 491 will be the creation of Verilog files using the Xilinx ISE software package. Because ISE does not work well with network drives your working Verilog files should be placed in a directory on the "C" drive. **Be sure to back up your files regularly** from the C drive to your network drive account or another safe place to avoid losing your work.