

ECE 491

Laboratory 2 – Sequential FPGA Design with Verilog

September 10, 2007

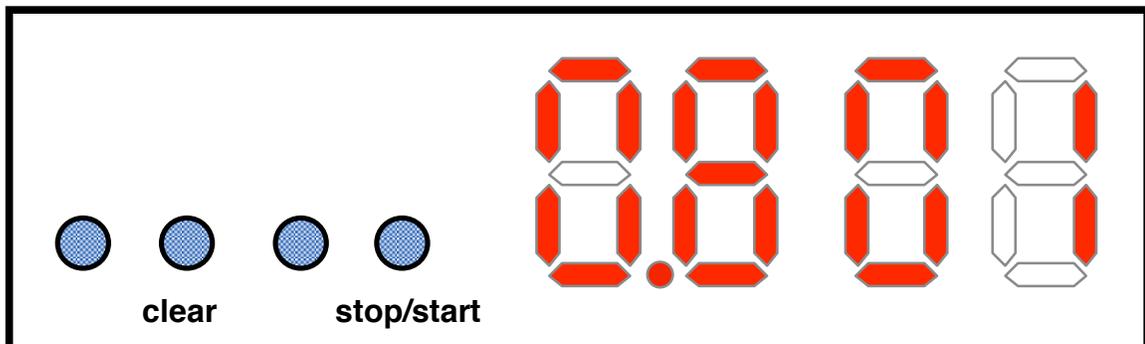
Goals

- To gain experience using Verilog for sequential logic design in FPGAs.
- To gain experience using parameterized modules in Verilog.
- To gain experience interfacing the FPGA to I/O devices on the Spartan 3 Starter Kit Board and to external signals via the board's edge connector.
- To design "building block" circuits that will be used in later laboratories.

Requirements

You will design the following sequential digital circuits:

1. Parameterized Counter – a counter parameterized by *radix* and *number of bits*. Counter will include a synchronous reset input, and enable input, and a carry output which is asserted when (i) the enable input is true and (ii) the current count value equals *radix-1*.
2. Clock Divider – a parameterized circuit that “divides down” a clock signal from an initial frequency (default 50MHz) to a desired frequency (default 1KHz) and produces a 50% duty-cycle clock waveform. All flip-flops in this circuit must be triggered by the input clock. The proper operation of your clock divider must be demonstrated in lab with an oscilloscope.
3. Seven-Segment Display Control – a circuit which has as input four 4-bit binary coded decimal (BCD) values and displays them on the 4-digit seven-segment display on the S3 Board. This circuit will operate by “time-multiplexing” the 7-segment LED output while changing which digit is enabled using the “digit_enable_out” output port. The display must not flicker excessively during operation.
4. Digital Stopwatch – a stopwatch that uses the buttons and 7-segment displays to implement the user interface shown below. It should count elapsed time from 0.000 to 9.999 seconds as controlled by the START/STOP pushbutton. A separate CLEAR pushbutton will set the stopwatch to 0.000 seconds.



Deliverables

1. Demonstration to Lab Instructor (using oscilloscope) of a working Clock Divider circuit that produces a 1KHz, 50% duty-cycle waveform.
2. Demonstration to Lab Instructor of working Digital Stopwatch circuit.
3. A short technical memorandum which describes (a) what was done, (b) what you learned, and (c) what difficulties you encountered.
4. Listings of all Verilog code used in the design. Each Verilog file should include a header block that includes your names, a description of what the file does, and (if derived from a previous design) credit to the creator of the original design file.
HINT: (use the "Edit->Templates" menu to quickly generate a header block template and fill it in with the specifics. These listings should be stapled to your Tech Memo.
5. Entries in your Lab Notebook documenting design ideas, the steps taken to create and debug your design, any pitfalls you encountered, and recorded data (if any). Each Lab Notebook entry should be dated and signed by all students in the lab group.

Additional Notes

1. The Spartan 3 Starter Kit board includes an on-board 50MHz clock signal. It is connected through the "clk" port in the top-level Verilog file "s3board.v". While this is a good clock rate for high-speed applications, it is often useful to create slower clock signals. This can be done using a *clock divider* circuit, which you will design as part of this lab. You can use your parameterized counter design to create a clock divider, but some additional work will be needed to guarantee a 50% duty cycle.
2. When using your clock divider, to drive a digital circuit, do not connect the clock divider's reset input to the reset input of the digital circuit. If you do, your circuit will never "see" the reset signal because the clock divider will stop generating clock edges while the reset input is asserted.
3. Be careful designing digital circuits that contain more than one clock. Ideally, each circuit should contain only one clock, but this is not always possible. When mixing clock signals, signals passing from one "clock domain" to another should be *synchronized* with a D flip-flop to control when the inputs change.
4. It is necessary that pushbutton switch inputs be *debounced* so that the mechanical "bouncing" that switches do when opened and closed is not interpreted as multiple button presses. You can use the file "debounce.v" available on the lab web page for this purpose. However, you must be sure to operate this circuit with a slow enough clock so that there is time for the bouncing input to settle.
5. It is often useful to connect an FPGA output directly to an external connection. The S3 Board has three edge connectors that connect FPGA pins to other boards, including the breadboard. We will use the "A2" connector to access some of these signals for debugging (and later in the class for building our network interface). These pins are documented in the *Spartan-3 Starter Kit Board User's Guide*, which is available in the DSP/VLSI lab (also from web – see the link on the ECE 491 Labs webpage). Each time an external output or input is used, a new port must be added to the top-level module "s3board.v". In addition, the constraints file "s3board.ucf" must be edited to associate the port with the proper pin(s) of the FPGA.

In this lab, you are required to verify the proper operation of your clock circuit by connecting it to an external pin. You can do this by adding a new output port to the top-level module called, say, "sclk" (for "slow clock"). Edit the constraints file to connect this port to FPGA pin E6. This will connect the output to pin 4 on the A2 edge connector of the S3 board (this pin is marked "PA38" on the breadboard).