An FPGA-Based Wireless Network Capstone Project

John A. Nestor Chris Nadovich
Department of Electrical and Computer Engineering
Lafayette College, Easton, Pennsylvania 18042
{nestorj, nadovicc}@lafayette.edu

Abstract

This paper describes a senior-level ECE capstone project in which students design, implement, and debug a wireless network using FPGAs with a small amount of attached circuitry. The project requires students to design the physical and media access control layers of a protocol based on IEEE 802.11, but simplified to make it feasible in a semester-long course. Specifically, the physical layer uses a VHF link with Bipolar Phase Shift Keying that can be implemented using the FPGA and a small analog front end. The protocol implements the basic Carrier Sense Multiple Access/Collision Avoidance mechanism of IEEE 802.11 while leaving out more advanced features. The resulting project requires that students learn the concepts of the design process, apply their knowledge of several different ECE topics, and implement a complex design.

1. Introduction

The *capstone project* has become an important part of engineering pedagogy. ABET Criterion 4 states that "students must be prepared for engineering practice culminating in a major design experience based on the knowledge and skills acquired in earlier course work and incorporating appropriate engineering standards and multiple realistic constraints" [1]. Several electrical and computer engineering (ECE) capstone courses have been described in the literature (e.g., [2-4]).

Creating a successful capstone course is challenging for a number of reasons. First, it is difficult to assign a project that is both substantial enough to be considered a "major design experience" and at the same time possible to complete in a single semester. Second, the project should build on the wide variety of topics in an undergraduate ECE curriculum, including digital design, electronics, communications, and electromagnetics. Finally, while prerequisite courses provide students with the technical skills needed to complete a capstone project, they often do not provide a background in the design process, project management, or the impact of external constraints such as cost, manufacturability, sustainability, and political and legal considerations.

This paper describes a capstone project that was developed at Lafayette College in which students design and implement a wireless network using FPGAs with a small amount of attached analog hardware. A wireless network is an attractive project because it includes aspects of all of the key subject areas of the ECE major. It also gives students exposure to economic, political, legal, and ethical constraints. An FPGA is an excellent platform for such a project due to its low cost, high functionality, and ease of programming using a hardware description language (HDL). The main limitation of the FPGA - that it can only implement digital logic - is addressed using an analog front end board that plugs into the FPGA board's edge connector.

This paper is organized as follows: Section 2 describes the organization of the course and project. Section 3 describes the wireless link used to implement the physical layer of the network protocol, while Section 4 describes the network protocol used, which is based on IEEE 802.11 [5] but simplified to make the project feasible in a single semester. Section 5 describes our experience with the project during its first use in Fall 2008. Section 6 concludes the paper and suggests future work.

2. Course and Project Organization

ECE 491 (Senior Design I) is the first of a two-course project sequence taken by ECE Seniors at Lafayette. In ECE 491, students work on a project in small groups of 2-3 while learning about the design process. ECE 491 is intended to be a bridge between

the supervised coursework of previous courses and a second, more open-ended team project in the following course, ECE 492 (Senior Design II).

The major goals of ECE 491 are to: 1) provide students with the skills to attack a significant FPGA-based project; 2) introduce students to the design process and the external constraints encountered in industrial design; and 3) introduce students to basic networking principles with emphasis on the physical and media access control layers.

The course is organized with lectures in the first eight weeks that address each of the three goals. First, students review FPGA-based design with Verilog and learn advanced design techniques, including verification. Students also learn the principles of data communications and networking, including the serial data transmission, Manchester codes, the OSI protocol stack, Ethernet, and IEEE 802.11. Lectures about the design process, project management, design reviews, intellectual property, and safety, environmental, and sustainability concerns are interspersed throughout the semester.

The laboratory portion of the course is divided into a set of eight experiments followed by a 6-week project period. The experiments expose students to design problems of increasing complexity with an emphasis on data communications and networking. Many of these experiments create modules that are later used as building blocks in the final project. For example, the last two experiments require students to design a Manchester Transmitter and Receiver that are key components in the network interface.

Both experiments and project use the Spartan-3 Starter Kit [6] FPGA board, which includes a Xilinx XC3S200 FPGA and provides an edge connector that is used to connect an analog front-end card.

3. Wireless Network – Physical Layer

The various IEEE 802.11 (a)-(n) standards transmit RF signals at frequencies ranging from 2.5GHz – 5GHz using either Orthogonal Frequency Division Multiplexing (OFDM) or Direct Sequence Spread Spectrum (DSSS) modulation techniques. Designs of this complexity are beyond the scope of a single semester capstone course and would require special circuitry to generate RF at the appropriate frequency.

To make the physical link more tractable, a simpler scheme is used which employs Bipolar Phase Shift Keying (BPSK) at a much lower frequency of 228.57134MHz. The carrier for this signal is generated directly by a Digital Clock Module (DCM) in the FPGA using the 50MHz clock provided by the FPGA board. BPSK requires that the transmitted signal phase be shifted 180° between a zero and one symbol. This is implemented using an exclusive OR gate. FPGA outputs drive a half-wavelength dipole antenna through a 300 Ω – 75Ω transformer. Figure 1 shows the basic structure of the transmitter.

The BPSK Receiver is more complex because it requires a Costas Loop [7]. However, most of the design can be realized in digital hardware on the FPGA. Figure 2 shows the analog front end, which converts the modulated RF to an Intermediate Frequency (IF) and samples the IF using a comparator. This circuit is constructed on a printed circuit board using parts that students are familiar with from their junior electronics courses. The front-end card plugs into an edge connector on the Spartan 3 FPGA board.

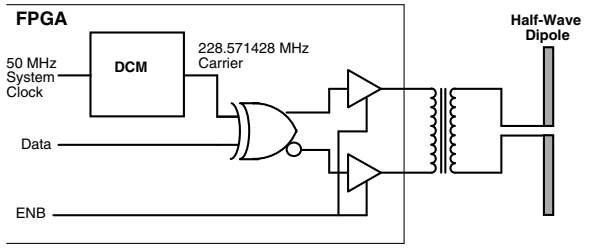

Figure 1 – BPSK Transmitter

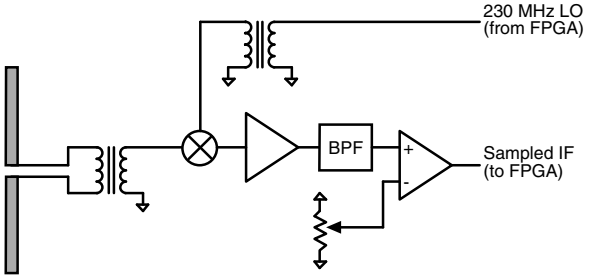

Figure 2 – BPSK Receiver – Analog Front End

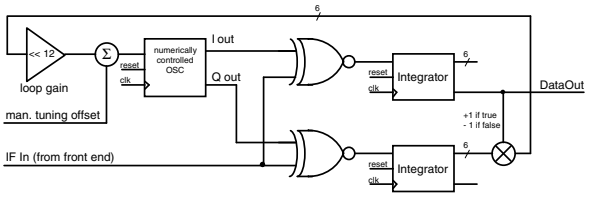

Figure 3 – BPSK Receiver – Digital Costas Loop

Figure 3 shows the block diagram of the digital Costas loop. The single-bit sampled IF from the analog front end feeds exclusive NOR gates that act as phase detectors by mixing the IF data with I and Q

signals from a numerically controlled oscillator. The mixer output feeds to two integrators, each of which generates an "amplitude" 6-bit output and a hard-limited, 1-bit "digital" output. The amplitude output of the Q channel integrator is fed back to a shifter that implements loop gain. After adding a manual tuning offset, this value drives the numerically controlled oscillator to complete to loop.

Figure 7 shows a photograph of the combined FPGA board and front end board, while Figure 8 shows the two boards connected to a half-wave dipole antenna.

4. Wireless Network – MAC Layer

The Media Access Control (MAC) layer of the simplified network is based on the Carrier Sense Multiple Access/Collision Avoidance (CSMA/CD) method employed by IEEE 802.11 [5]. Each team of students implements a wireless "station" with a unique 8-bit MAC address (reduced from 32 bits in 802.11) that transmits and receives *frames* (packets) of data to and from other stations.

The project requirements specify four different frame types in the format shown in Figure 4. Each frame type is transmitted serially using the Manchester Code. Type 0 frames are used for basic transmission from station to station without error checking or acknowledgement and contain preamble, destination, source, type, and data fields. Type 1 frames require an additional Frame Check Sequence (FCS) field that is used to detect transmission errors. Type 2 frames require that the receiving station transmit a Type 3 "acknowledge" (ACK) frame back to the sending station to indicate success. Project grading is weighted to encourage students to get basic transmission of Type 0 frames working first before attempting more advanced features.

Since collisions cannot be sensed in a wireless environment, the 802.11 standard calls for the use of a *Distributed Coordination Function* (DCF) in which stations perform *Collision Avoidance*. Figure 5 shows how the DCF approach is used to transmit a frame. A station that is ready to transmit must first wait until it senses no transmission from other stations and then wait for a time interval specified by a Distributed Interframe Spacing (DIFS) interval followed by a random number of delay "slots" before beginning transmission. The use of the random delay reduces the probability that two stations will transmit at the same time and cause a collision.

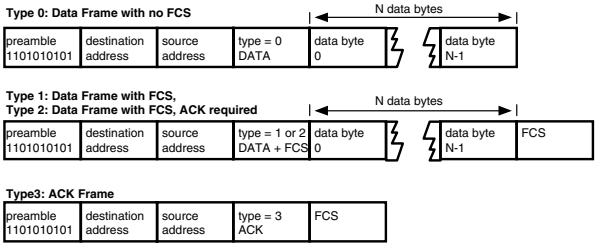

Figure 4 – Network Frame Formats

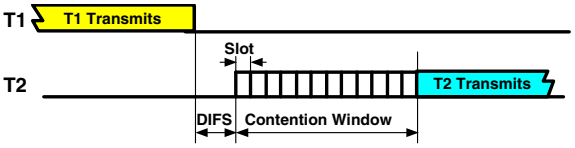

Figure 5 – Basic Frame Transmission

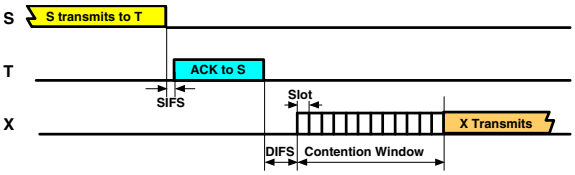

Figure 6 – DCF with ACK (Acknowledge) Frame

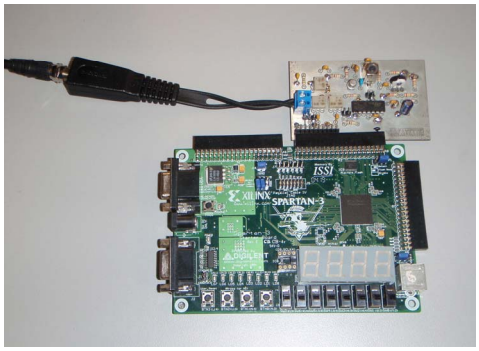

Figure 7 – FPGA Board with Analog Front End

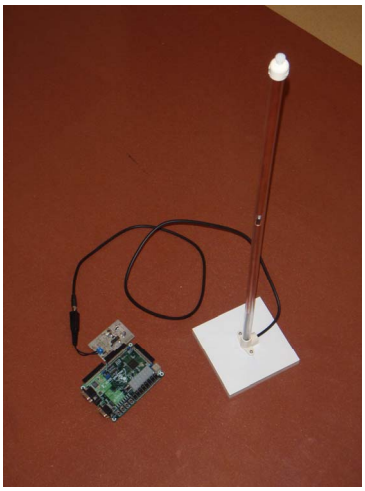

Figure 8 – FPGA Board, Front End and Antenna

Type 2 and 3 frames implement a handshake to indicate to a transmitting station that a frame has been received, as shown in Figure 6. If the sending station S sends a Type 2 frame to station T, it expects to receive an ACK frame back from station T after a Short Interframe Spacing (SIFS) interval. If the ACK frame is not received in a specified timeout interval, S must attempt to retransmit the frame up to a maximum number of retry attempts. More advanced 802.11 features such as Request to Send/Clear to Send are not required to reduce project complexity.

5. Results

The wireless network capstone project was used in two sections of ECE 491 in Fall 2008. Final project grading was based on the completion of a preliminary design which was evaluated in a design review, compliance with requirements in the project assignment (including safety, environmental, and IP constraints), verification, and a demonstration of working transmission of each different frame type.

Table 1 shows the outcome of the project in terms of the features completed by each group. For each frame type, an "S" indicates that the design could successfully send a frame of that type, while an "R" indicates that the design could receive a frame of that type. All but one group successfully demonstrated transmission with basic Type 0 frames, which is not surprising since these are the most basic form of transmission. Roughly half the groups demonstrated Type 1 frames (with a FCS field), while only two groups were able to partially or fully demonstrate the more complex handshake required by Type 2 and Type 3 frames.

Student response to the project has been positive. Comments on course evaluations indicated that students found the project interesting and challenging but suggested that the workload be distributed more evenly through the semester. Based on these comments the lab experiments leading up to the project have been reorganized to provide students with more time during the project. Student evaluations for the overall course showed a significant improvement over the previous year's course in which students designed a wired network.

As part of the course outcomes assessment, students were surveyed with regard to their confidence that the course's objectives had been achieved. This survey showed strong confidence overall that the outcomes were achieved, but also indicated areas where improvement is needed, including design team organization, project management tools, dealing with complex constraints, avoiding Verilog coding pitfalls, and timing and synchronization. Coverage of these topics will be increased in the future.

6. Conclusion

This paper has described an ECE capstone course in which students design a wireless network using an FPGA with an attached analog front end. This project allows students to apply their knowledge of many different ECE topics while learning how to complete a significant design project.

A number of improvements could be made to this project. First, the lecture material could be enhanced with a more in-depth review of RF modulation techniques to give students a better appreciation of the transmitter and receiver circuits. Second, the design of the analog front end could be improved to increase the receiver's sensitivity. Finally, more advanced features could be included in the network interface to make the project more challenging.

References

[1] Accreditation Board for Engineering and Technology, "Criteria for Accrediting Engineering Programs", November 2008. Available: http://www.abet.org.

[2] R. H. Klenke, "Experiences Using the Xilinx Microblaze Softcore Processor and uCLinux in Computer Engineering Capstone Senior Design Projects", *Proceedings MSE Conference,* pp. 123-124, June 2007.

[3] D. J. Jackson and K. Ricks, "FPGA-Based Autonomous Vehicle Competitions in a Capstone Design Course", *Proceedings MSE Conference*, pp. 9-10, June 2005.

[4] A. Saad, "Senior Capstone Experiences for ABET Accredited Electrical and Computer Engineering Education", *Proceedings IEEE Southeastcon*, pp. 294-299, March 2007.

[5] B. O'Hara and A. Petrick, *IEEE 802.11 Handbook: A Designer's Companion*, 2nd ed. IEEE Press, 2005.

[6] Xilinx Corp, *Spartan 3 Starter Kit Board User Guide*.

[7] J. Feigin, "Practical Costas Loop Design", *RF Design*, pp. 20-36. January 2002.

Lab Group (Size)	Type 0	Type 1	Type 2/3
Group 1 (2)	SR		
Group 2 (2)	SR		
Group 3 (2)	SR	SR	
Group 4 (3)	SR	R	
Group 5 (2)			
Group 6 (2)	SR	SR	
Group 7 (2)	SR		
Group 8 (2)	SR	SR	S
Group 9 (2)	SR	S	
Group 10 (2)	SR	SR	SR

Table 1 – Project Completion Data